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09/410,646	10/01/1999	DAVID A. EDWARDS	99-TK-262	7191

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EXAMINER
MASKULINSKI, MICHAEL C

ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/410,646	Applicant(s) EDWARDS ET AL.
	Examiner Michael C Maskulinski	Art Unit 2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 17-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 16, two circuits are claimed—the overall circuit and a circuit for monitoring. This makes it difficult to determine which circuit is being referred to in claims 17-23. Referring to claim 17, the examiner is unsure as to what circuit is the integrated circuit and will interpret it as being the overall circuit. Referring to claims 18 and 19, the examiner understands the circuit being referred to as being the circuit for monitoring. Referring to claims 20-23, the examiner understands the circuit being referred to as being the overall circuit. For the rest of the Office Action, the claims will be interpreted in this manner.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of co-pending Application No. 09/410,642. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 1 of the present invention is drawn to a circuit for monitoring information put onto an interconnect by one or more modules, said circuit comprising circuitry for determining if the information on the interconnect matches one or more conditions; and circuitry from preventing a module from putting further information onto said interconnect if it is determined that information on the interconnect matches said one or more conditions. However, claim 1 doesn't have circuitry for receiving at least part of said information. Claim 5 of co-pending Application No. 09/410,642 is drawn to a system comprising an interconnect and a plurality of modules connected to said interconnect for putting information onto the interconnect, a circuit comprising: circuitry for receiving at least part of said information; circuitry for determining if said at least part of information satisfies one or more conditions; and circuitry for performing an action to prevent one or more modules from being granted access to the interconnect in response to the determination that at least part of the information satisfies one or more conditions. It would have been obvious to one of ordinary skill at the time of the invention to include circuit of co-pending Application 09/410,642 into the present Application. A person of ordinary skill in the art would have been motivated to make the

modification because it is well settled that the omission of the circuitry for receiving at least part of said information is an obvious expedient if the remaining elements perform the same function (In re Karlson, 136 USPQ 184 (CCPA 1963).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 7-9, 11-14, 16, and 18-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolff et al., U.S. Patent 4,486,826.

Referring to claims 1, 16, 25:

a. In column 2, lines 31-35, Wolff et al. disclose a computer system, which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module.

b. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations

within each unit and check information transfers between the units (circuitry for determining if the information satisfies one or more conditions).

c. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for preventing a module from putting further information onto said interconnect in response to the determination that the information satisfies one or more conditions).

Referring to claims 2 and 3, in column 3, lines 57-68, Wolff et al. disclose that the bus carries cycle-definition (type of transaction to which the information relates), address (address of the information), data, parity, and other signals that can be compared to warn of erroneous information transfer between units (match conditions). The information comprising packets of information, requests, and response is inherent to the information mentioned above that is sent over a bus.

Referring to claim 7, in column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (prevent one or more modules from being granted access to the interconnect). Further, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a broken flip-flop (preventing circuitry) to disable the drivers of a peripheral device in response to a fault.

Referring to claim 8, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control

section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 9 and 11, in column 25, lines 32-40, Wolff et al. disclose that the central processing unit (circuit) has two subsystems and control circuits within the unit that take the unit off-line upon detection of an error (precondition: enabled or not enabled). Further, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (preventing circuitry).

Referring to claims 12 and 13, in figures 5A, 5B, and 1, and in column 28, lines 21-35, Wolff et al. disclose latch 120 which is between the interconnect and the processor module (circuitry external to said circuit). The latch provides temporary storage of output data so that in the event any error is reported on the buses, the operating sequence in which the error was reported can be duplicated and the data retransmitted on the A bus 42 (external circuitry is enabled).

Referring to claim 14, in column 3, lines 57-68, Wolff et al. disclose that the bus carries cycle-definition (type of transaction to which the information relates), address (address of the information), data, parity, and other signals that can be compared to warn of erroneous information transfer between units (match conditions). The

information comprising packets of information, requests, and response is inherent to the information mentioned above that is sent over a bus.

Referring to claim 18, in column 20, lines 35-55, Wolff et al. disclose an arbitration network (arbiter) which provides an automatic hardware determination of which unit, or pair of partner units, that requests access to the bus structure (interconnect) has priority to initiate an operating cycle (granted access). In column 3, lines 34-47, Wolff et al. disclose that upon detection of an error-manifesting fault in any unit, that unit is isolated and placed off-line so that it cannot transfer information to other units of the module (preventing circuitry). As stated above upon detection of an error in a unit, that unit is isolated and taken off-line, therefore, the unit cannot participate in the arbitration (module prevented from putting information onto the interconnect is prevented from winning an arbitration).

Referring to claim 19, in column 20, lines 35-55, Wolff et al. disclose that the processor module (determining circuitry) has two arbitration networks (arbiter) connected to bus A and bus B.

Referring to claim 20, in the abstract, Wolff et al. disclose a bus.

Referring to claims 21, 22, and 23, in column 2, lines 48-63, Wolff et al. disclose error detectors (debug module) at the level of each functional unit (module). Further, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator, which switches a so-called broken flip-flop to disable the drivers upon detection of an error (preventing circuitry). The comparator is part of the control unit, which is part of the functional unit (determining circuitry in said debug module).

Referring to claim 24:

a. In column 2, lines 31-35, Wolff et al. disclose a computer system, which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure (interconnect) which provides all information transfers between the several units of the module.

b. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for preventing a module from putting further information onto said interconnect).

c. In column 20, lines 35-55, Wolff et al. disclose an arbitration network (arbiter) which provides an automatic hardware determination of which unit, or pair of partner units, that requests access to the bus structure (interconnect) has priority to initiate an operating cycle (granted access). In column 3, lines 34-47, Wolff et al. disclose that upon detection of an error-manifesting fault in any unit, that unit is isolated and placed off-line so that it cannot transfer information to other units of the module (preventing circuitry). As stated above upon detection of an error in a unit, that unit is isolated and taken off-line, therefore, the unit cannot participate in an arbitration (module prevented from putting information onto the interconnect is prevented from winning an arbitration).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S Patent 4,486,826 as applied to claim 6 above, and further in view of Cepulis et al., U.S. PGPub 2001/0042225 A1.

Referring to claim 4, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a so-called broken flip-flop to disable the drivers of a peripheral device (module) in order to prevent it from putting further information onto the bus (interconnect). However, Wolff et al. don't explicitly disclose using a register for preventing a module from putting information onto the interconnect. In paragraph 0019, Cepulis et al. disclose a fault detection and isolation technique that tracks failed physical devices by identification (ID) codes embedded in particular computer components. It would have been obvious to one of ordinary skill at the time of the invention to include the identification codes of Cepulis et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because *to ensure proper operation in the event of a failed component, the computer system must be capable of (1) detecting the failure, and (2) isolating the failed component so it is no longer accessed* (Cepulis et al.: paragraph 0007). One way to isolate a failed

component is *to maintain a list of failed logical devices in a "failed device log"* (Cepulis et al.: paragraph 0013).

Referring to claim 5, in paragraph 0039, Cepulis et al. disclose that the FDL (failed device log) entry to identify a failed physical device may include setting a bit in the FDL corresponding to the failed device.

Referring to claim 6, in paragraph 0036, Cepulis et al. disclose that generally a computer system identifies a device that has failed using its unique ID code rather than the logical address associated with that physical device (the location being independent of the address of the module).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 13 above, and further in view of Ardini, Jr. et al., U.S. Patent 4,918,693. In column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator). However, Wolff et al. don't explicitly disclose satisfying a precondition by having match conditions occurring a predetermined number of times. In column 8, lines 9-14, Ardini, Jr. et al. disclose a diagnostic program that, after a certain number of parity error signals are received from board 202, it will send a code to disable the parity check circuit output. It would have been obvious to one of ordinary skill at the time of the invention to include the parity error signal threshold of Ardini, Jr. et al. into the system of

Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because a parity check circuit can become faulty so that it continuously generates a parity error signal on its output (see Ardini, Jr. et al.: column 8, lines 7-9). In this case, to check for a faulty parity circuit would require a precondition.

10. Claim 15/1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 1 above, and further in view of Pizzica, U.S. Patent 5,652,754. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions). However, Wolff et al. don't explicitly disclose storing circuitry to store the information which satisfies the at least one condition. In column 2, lines 53-60, Pizzica discloses a signature storage device that stores a fault free signature from a functional digital module and faulty signatures obtained by shorting and opening each of the circuit nodes thereof. It would have been obvious to one of ordinary skill at the time of the invention to include the faulty signature storing of Pizzica into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because *the recorded signatures can be used for subsequent pass/fail determination of digital modules that are tested* (see Pizzica: column 1, lines 46-48).

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 22 above, and further in view of

Bershteyn et al., U.S. Patent 5,678,028. In the abstract, Wolff et al. disclose a fault-tolerant computer system comprising a processor unit, a memory unit, one or more peripheral control units, and a bus structure. However, Wolff et al. don't explicitly disclose that these circuits are an integrated circuit. In the Background of Bershteyn et al., a system-on-a-chip debugger is disclosed. It would have been obvious to one of ordinary skill at the time of the invention to make the system of Wolff et al. into the system-on-a-chip debugger of Bershteyn et al. into the. A person of ordinary skill in the art would have been motivated to make the modification because an entire system can be fabricated on a single wafer decreasing the cost of the entire system (see Bershteyn et al.: column 1, lines 45-67).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

In U.S. Patent 5,361,347, Glider et al. disclose a resource management in a multiple resource system where each resource includes an availability state stored in a memory of the resource.

In U.S. Patent 6,000,043, Abramson discloses a method and apparatus for management of peripheral devices coupled to a bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Mon-Thu 7:30-5 and Fri. 7:30-4 (second Fri.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3718 for regular communications and (703) 305-3718 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MM
May 2, 2002

Scott Baderman
Primary Examiner
Art Unit 2184